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Hybrid FDTD Large-Signal Modeling of Three-Terminal Active Devices

Qiang Chen and V. F. Fusco

***Abstract*—A general algorithm for including large-signal active three-terminal models into the finite-difference time-domain (FDTD) method is presented. A dynamic interface between the active device and the FDTD lattice is used to simulate the prominent nonlinear time-dependant behavior of the three-terminal active device, which is connected across multiple FDTD cells. A technique for introducing an internal electromagnetic (EM) field absorber into the FDTD three-terminal active device model in order to eliminate undesired current coupling is discussed. Numerical comparison shows this method is accurate and expected to have general utility for other complicated hybrid lumped-circuit FDTD modeling situations.**

***Index Terms*— Active devices, finite-difference time-domain method, large-signal models.**

I. Introduction

Lumped-element modeling is a very important aspect for the future development and application of the finite-difference time-domain (FDTD) method [1]–[7]. It is well accepted that a lumped element can be represented by lumped-current(s) in the FDTD algorithm. To accurately represent a general lumped-element case, this lumped-current should satisfy two requirements.

1) It should be connected across multiple, rather than (as at present) single, FDTD cells so that an arbitrarily sized lumped element can be modeled.
2) A dynamic interface between the FDTD electromagnetic (EM) fields and the lumped element's *I–V* behavior (i.e., the lumped-current) should be calculated using the present, rather than the former, time-step of the discretized EM field in such a way that the obtained lumped-current is correct for both the FDTD EM-field computation and the lumped-element *I–V* characteristic at any given time-step.

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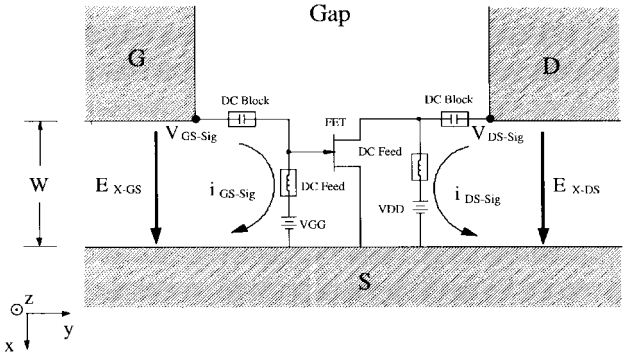

Fig. 1. Interface region between FDTD solver field and three-terminal device model.

The first above-mentioned requirement was recently addressed by Durney *et al.* [5] and the second by Piket-May *et al.* [6], where a semi-implicit average of present and former time-step values was used. However, due to numerical complexities involved, these two aspects have not been accounted for concurrently. The parametric technique [7] is an attempt to take these two requirements simultaneously into account. The technique is simple and accurate for simple lumped-elements, i.e., a resistor, a capacitor, a diode, etc. However, for complicated lumped-element circuits, it is difficult to simulate their behavior by the method of media parameters variation. In this paper, an FET connected across a unilaterally gapped slotline (Fig. 1) is taken as an example of a general method for lumped-element modeling. Since the FET large-signal model is indeed a complex three-terminal nonlinear lumped-element circuit containing passive, source, and control elements, the method presented here is expected to be useful for any other lumped-element/circuit models. In addition, in this paper, the decoupling between the lumped gate current and lumped drain current in the FET FDTD model is discussed.

II. Interface Between Slotline Field and FET Model

Table I shows the parameters of a general packaged large-signal FET model,[1] [8] customized for the NE72089 device to be included into the FDTD algorithm. Its nonlinear port (source and drain) currents can be calculated by time-domain analysis by solving a set of differential equations provided the port voltages are known. Thus, the obtained lumped currents are then used in the FDTD algorithm for the interaction of FDTD EM fields and the FET behavior. Fig. 1 shows the port voltages and port currents as an interface between the distributed fields and the FET model in the slotline example. The unilateral slotline gap between the source and drain of the FET is for dc bias. From the figure, it can be seen that dc-bias voltages are applied and simulated directly in the FET model. Thus, only signal fields (with no dc bias) are analyzed by the FDTD method in the slotline. This simplifies the FDTD simulation and gives an advantage for any further circuit simulation using the hybrid field. For the simulation of other circuits with a high level

[1] HP 85150B Microwave and RF Design Systems, *Microwave Library Components (Lumped, Ideal, & Nonlinear)*, ch. 17, vol. 4, Component Catalog, Hewlett-Packard Company, 1994.

TABLE I
PARAMETERS OF A LARGE-SIGNAL NE72089 FET MODEL

IDS Curtice model	Gate model	Parasitics	Breakdown	Package
vt0=-1.17 V	rgs=15.3 Ω	rg=1 Ω	gsfwd=2	cin=6.77×10^{-2} pF
beta=3.04×10^{-2}	gscap=2	rd=0.1 Ω	gdrev=2	cf=1.79×10^{-2} pF
lambda=4.88×10^{-2}	cgs0=0.774 pF	rs=6 Ω	vbi=0.8 V	cin=3.36×10^{-2} pF
alpha=2.39	gdcap=2	lg=0.991 nH	is=10^{-14}	
tau=10 ps	cgd0=0.153 pF	ld=0.666 nH	n=1.1	
	FC=0.5	cds=0.213 pF		

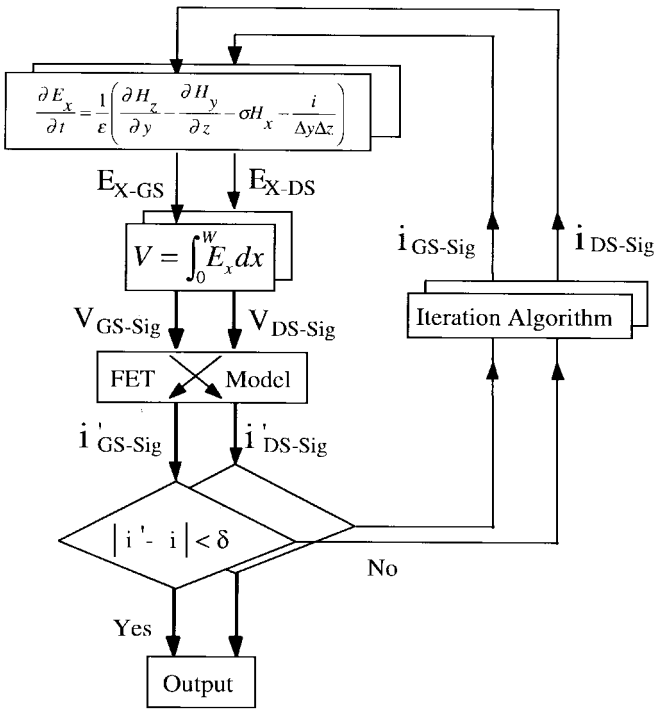

Fig. 2. FDTD-field and FET-model interface analysis at each time-step; δ is the minimum precision requirement.

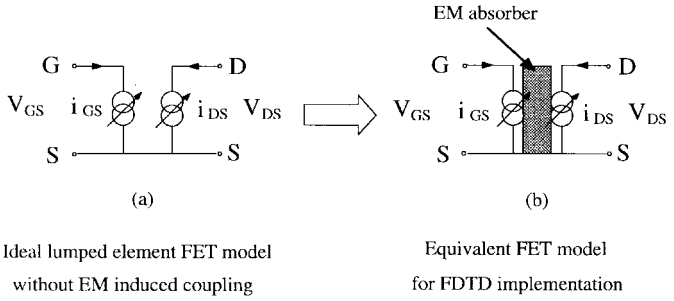

Fig. 3. An equivalent FET model for FDTD simulation.

of interaction among various elements, dc bias inclusion might be required. This will increase the computation effort considerably. The electrical fields at the lumped-element position are calculated using Maxwell's equations. As an example, at the position where an x-directed lumped-current ($i_{\text{GS-Sig}}$ or $i_{\text{DS-Sig}}$) is located (Fig. 1), the E_x-field component equation is given in Fig. 2. Using a central-difference formula at time-step $(n + 1/2)$ and spacial grid (i, j, k), a discretized FDTD iteration formula of the equation can be obtained. The signal voltage at the gate or drain port is obtained by integration of E_x over the slot width W (see Fig. 1). Then the obtained $V_{\text{GS-Sig}}$ and $V_{\text{DS-Sig}}$ are fed into the FET model where the port current $i_{\text{GS-Sig}}$ and $i_{\text{DS-Sig}}$ are obtained. These currents are then compared with the original currents in the Maxwell-equation solution. If their absolute difference values do not satisfy previously defined accuracy requirements, a Newton iteration method is used to locate the correct values. Fig. 2 shows the procedures which are executed at each time-step. The inner loop in Fig. 2 is the drain voltage/current computation loop. It takes the gate voltage and current values from the outer loop, which is the gate voltage/current computation loop. These two loops are interlinked to each other by the FET-model intrinsic coupling. In this way, a lumped element connected across any number of grid cells can be accurately modeled at each time-step. Since only the FDTD cells occupied by the gate and drain currents are involved, and only a few nonlinear element values in the FET model need to be updated in the lumped-current value computation shown in Fig. 2, the computation time required is very small when compared with the FDTD iteration routine at each time-step. Also, because the present time-step current values are computed based on accurately obtained previous time-step values, the convergent speed for present time-step current computation is quite high. It has been found that in this paper's large-signal FET model application, the explicit and semi-implicit method described in [1], [6] are not applicable due to the integral calculation of lumped-element voltages across multiple cells. Also, if the present time-step currents are approximated by previous time-step values so as to save the iteration procedure for accurate current-value computation, numerical errors can accumulate quickly and lead to instability.

III. LUMPED-CURRENT DECOUPLING

As described above, an FET model can be simplified as two lumped currents, i.e., the gate current i_{GS} and drain current i_{DS} [see Fig. 3(a)], which are linked together solely through the mathematical expression of the FET lumped-circuit model. The interface analysis shows how the values of these two currents are calculated so that they accurately represent the FET gate and drain currents under device operational conditions. In the lumped-current model shown in Fig. 3(a), there is additional EM coupling between gate and drain currents. However, since the FDTD algorithm is a distributed-parameter EM simulator, this model is difficult to implement due to the strong EM coupling through the FDTD cells between the two currents since they are physically near to each other. This problem, in fact, represents the dilemma of expressing an internal lumped-circuit coupling mechanism in a distributed-parameter environment. In this paper, the simplified FET model [Fig. 3(a)] is modified into

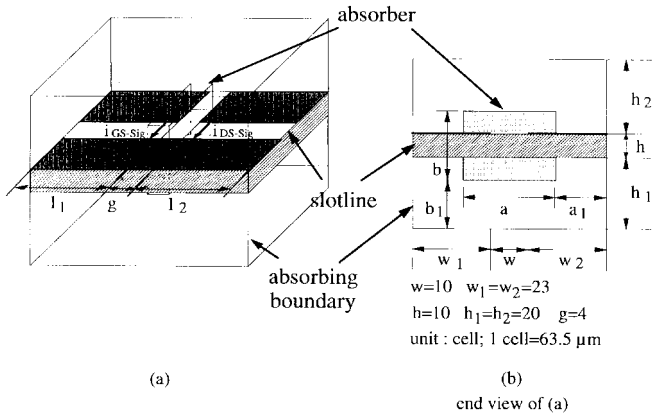

Fig. 4. An EM-field absorber in the FDTD FET modeling. (a) Width. (b) Height.

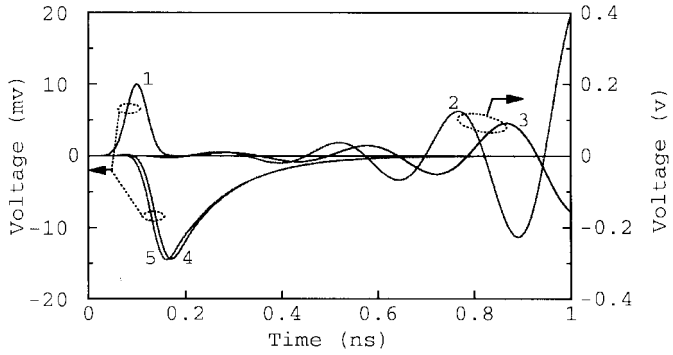

Fig. 5. Decoupling effect of different-sized absorber in the FDTD FET model. Curve 1 is the input Gaussian voltage. Curve 2 is the output FET drain voltage with no absorber, which shows strong FET self-oscillation. Curve 3 is the drain voltage with an absorber size of $a = 36$ cells, $b = 30$ cells, which still shows some gate and drain coupling. Curve 4 is the drain voltage with an absorber size the same as the cross-section plane of the slotline FDTD computation domain where the gate and drain coupling is eliminated. Curve 5 is the drain-voltage result from a time-domain differential analysis of the FET large-signal model.

an equivalent form suitable for FDTD implementation, as shown in Fig. 3(b). An EM absorber is inserted between the gate and the drain so that they are electromagnetically separated when applied into the FDTD lattice. This modified model has the same physical meaning and mathematical expression as Fig. 3(a). The only difference is that it is EM-simulator oriented. Here, modified-dispersive absorbing-boundary conditions [9] are applied to the surface of the absorber. Fig. 4 shows the application of such an FDTD-oriented FET model connected across a gapped slotline. The thickness of the absorber is the same as the width of the gap, which is four cells in this case. The width [Fig. 4(a)] and height [Fig. 4(b)] of the absorber are made variable so that the effect of this numerical absorber can be examined (see Fig. 5). It can be concluded from Fig. 5 that the gate– and drain–current coupling is very strong in the FDTD FET model if no EM-field absorber is used between them. To eliminate this coupling from the FET FDTD modeling, a large-size absorber has to be used. In this paper, an absorber with the same cross-section size as that of the slotline FDTD computation domain, i.e., $a = w_1 + w + w_2$ and $b = h_1 + h + h_2$, is used to eliminate the undesired gate–drain coupling. It is understood that the insertion of a local absorber can affect the EM propagation close to the FET. However, compared with the dominant FET effects, EM-propagation effects around the device appear to be relatively weak. This issue will be verified in the following numerical discussion.

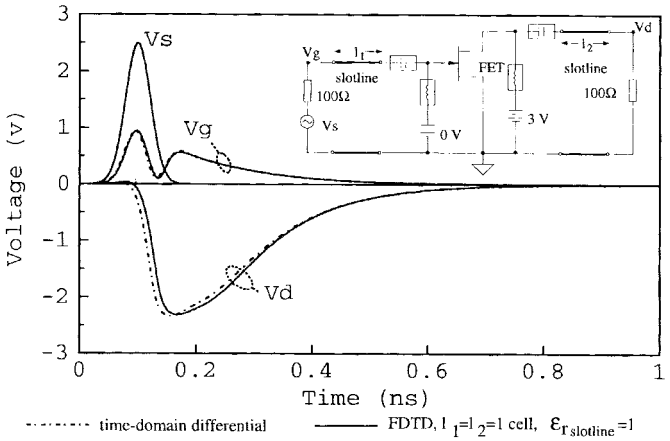

Fig. 6. Large-signal numerical result comparison (all the other dimensions of the unilaterally gapped slotline are shown in Fig. 4).

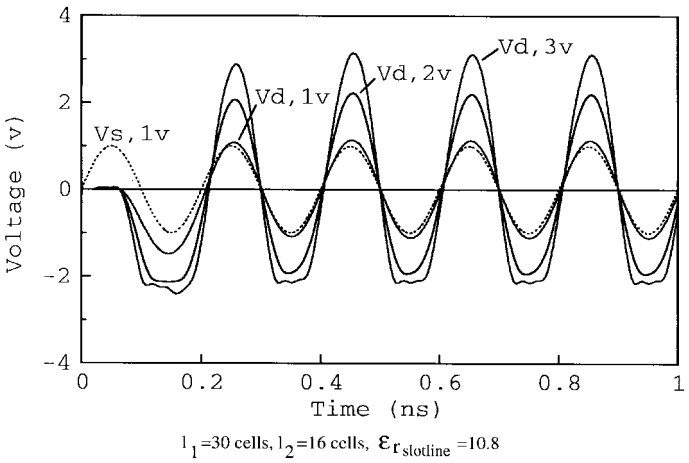

Fig. 7. Large-signal numerical results of the FET under different amplitude 5-GHz sine-wave excitation. Drain-voltage curves corresponding to different source signal amplitude are shown. A 1-V source signal is shown for phase reference (all the other dimensions of the unilaterally gapped slotline are shown in Fig. 4).

IV. Large-Signal Numerical Results

Fig. 6 illustrates large-signal numerical results. In this figure, this paper's FDTD FET modeling, and the time-domain differential FET-model analysis under a 2.5-V Gaussian-source excitation, are compared. In order to do this comparison, the relative dielectric constant of the slotline substrate is set to be 1 in the FDTD analysis. Also, the length of the interconnected slotline is set to the minimum values of one cell only. The two gate–voltage curves agree very well. The FDTD drain-signal voltage curve is slightly retarded with respect to the analytic one, due to the one-cell slotline interconnection. Fig. 7 shows the nonlinear characteristics of the FET under large-signal excitation. The average computation time for one curve in this numerical example is 130 min on a Sun Sparc station 5 computer. It can be seen that when compared with the reference source signal, there is little distortion to the drain-voltage curve of 1-V sine-wave excitation after it reaches steady state. With the increase of the source signal amplitude, the output drain voltage becomes more distorted due to the FET *I–V* feature. When the source amplitude is 3 V, the distortion becomes more obvious. This paper's method has been applied to the analysis of an active FET slot-ring antenna where the numerical prediction of oscillating frequency is confirmed to

within 1.6% by measurement [10]. These verify the accuracy of the large-signal FET FDTD modeling algorithm presented in this paper.

V. Conclusion

In this paper, a general algorithm for including large-signal active three-terminal models into the FDTD method is presented. A dynamic interface between the active device and the FDTD lattice is used to simulate the prominent nonlinear time-dependant behavior of the three-terminal active device, which is connected across multiple FDTD cells. A technique for introducing an internal EM-field absorber into the FDTD three-terminal active-device model in order to eliminate undesired current coupling is discussed. Numerical comparison shows this method is accurate and is expected to have general utility for other complicated hybrid lumped-circuit FDTD modeling situations.

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Resonance in a Cylindrical–Triangular Microstrip Structure

Kin-Lu Wong and Shan-Cheng Pan

***Abstract*—Full-wave solutions for the complex-resonant frequency of a triangular microstrip patch printed on a cylindrical substrate are presented. Curvature effects on the complex-resonant frequency, as well as the quality factor of the cylindrical–triangular microstrip structure, are analyzed. Measured resonant frequencies are also shown for comparison. Good agreement between measured and theoretical results is obtained.**

***Index Terms*—Microstrip antenna, microstrip resonator.**

I. Introduction

Characteristics of triangular microstrip structures used as resonators [1] or radiators [2], [3] have been reported. Results have shown that, as a resonator, the triangular microstrip structure at its fundamental mode (TM_{10} [1]) has a lower radiation loss than the circular microstrip resonators. It is also reported that, compared to the rectangular microstrip patch antenna, the microstrip antenna with a triangular patch is physically smaller and has similar radiation properties [2]. It is also noted that the related studies are mainly of planar geometries, and very scant results for the triangular microstrip patch mounted on a cylindrical substrate are available. This kind of cylindrical microstrip structure has the advantage of conformability and can find applications on curved surfaces such as those of aircraft and missiles.

In this paper, the theoretical analysis of the cylindrical–triangular microstrip structure is performed using a full-wave formulation. A basis function similar to the true current distribution on the patch surface is also selected for efficient and accurate numerical calculation. Numerical results for the complex-resonant frequencies [4], [5] of the microstrip structure are presented and discussed, and the quality factor of the microstrip structure is also analyzed. Measured resonant frequencies are also shown for comparison.

II. Theoretical Formulation

Fig. 1 shows the geometry of a cylindrical–triangular microstrip structure. The radius of the ground cylinder is a, and the cylindrical substrate has a thickness of h and a relative permittivity of ε_r. The sidelength of the triangular patch in the ϕ direction is d_2 $(= 2b\phi_0)$, and the other two sides are assumed to have the same length of d_1. The relationship of d_1 and d_2 is given by

$$d_1 = \sqrt{(d_2/2)^2 + (2z_0)^2} \tag{1}$$

where $2z_0$ is the distance from the tip of the triangle to the bottom side of the triangle.

To begin with, the full-wave formulation in [4] is followed, and the following equation is obtained:

$$\begin{bmatrix} \tilde{E}_\phi(n,k_z) \\ \tilde{E}_z(n,k_z) \end{bmatrix} = \overline{\overline{Q}}(n,k_z) \cdot \begin{bmatrix} \tilde{J}_\phi(n,k_z) \\ \tilde{J}_z(n,k_z) \end{bmatrix} \tag{2}$$

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